ELECTRO-THERMAL TRANSIENT SIMULATION OF SILICON CARBIDE POWER MOSFET

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Abstract

This research illustrates the transient performance of N-channel silicon carbide (4H-SiC) power MOSFET rated for a blocking voltage of 1200V and drain current density of 100A/cm^2. The simulation of vertical D-MOSFET half cell structure was performed at room temperature of 300K. The 2D device model was created and simulated using Silvaco© ATLAS Technology Computer-Aided Design (TCAD) physics based simulation software. Physics based models were used to accurately model electrical device parameters including carrier mobility, recombination effects, bandgap narrowing, impact ionization and lattice heating.

I. INTRODUCTION

Silicon Carbide has been a material of interest for power device fabrication due to its stability in extreme operating conditions including high ambient temperature. This robust nature of the material is primarily due to its wide energy bandgap, critical electric field and thermal conductivity [1]. To analyze the thermal stress on a power device, the device is simulated using DC steady state and transient conditions. Since power devices are mainly used in switching application, it is important to understand the thermal effects on the device and its electrical parameters when the device is switched on/off. This includes the thermal stress on the device, formation of hot spots and variation in mobility due to temperature change. During transient conditions, the device conducts for short time intervals which results in the generation of heat in the device lattice. If the switching frequency is high, the heat eventually gets dissipated to the ambient. However, during a single switching pulse or few switching pulses, the heat generated does not get transferred properly to the heat sink and has to be dissipated in the semiconductor material. This can lead to the formation of thermal hot spots within the material and subsequent device failure. The situation becomes really critical when the device operates at elevated ambient temperature conditions at high power levels.

II. DEVICE DESIGN

A. Mesh Design

In order to simulate a device using ATLAS TCAD, the device must be first modeled on to a 2D grid which is divided into grid/mesh points. In order to resolve space charge variations, the mesh size has to be smaller than the Debye length of the semiconductor which is defined as the distance in a semiconductor over which local electric field affects distribution of free charge carriers [2]. Considering the tradeoff between simulation accuracy and numerical efficiency, the device grid is designed in such a way that the mesh is fine in the critical regions of the device and coarse in the non-significant regions of the device like the substrate in case of power devices. Critical regions in a semiconductor device include areas of considerable recombination effects, high electric field or impact ionization, metal semiconductor junctions (e.g. in a schottky diode) and area under the gate oxide in a MOSFET [3]. Fig. 1 shows the mesh profile for the half cell D-MOSFET structure indicating the critical regions.

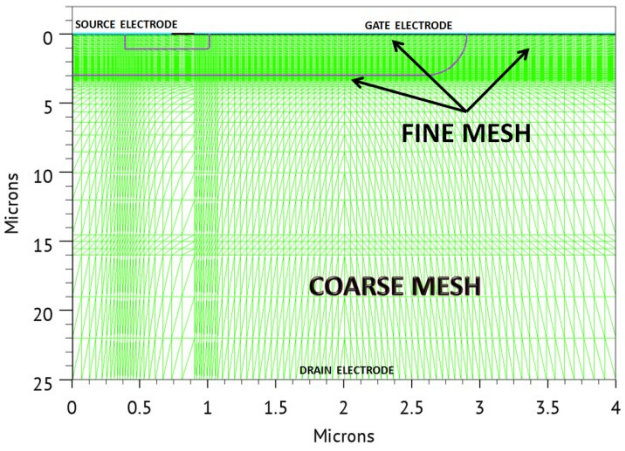

Figure 1. D-MOSFET half cell mesh profile.

B. Doping Profile

The MOSFET cell was designed for a blocking voltage of 1200V and a drain current density of 100A/cm^2. Unlike the parallel plane breakdown voltage, in case of a MOSFET, due to edge terminations, the breakdown voltage is related to the parallel plane breakdown voltage (BV_{PP}) via the following equation [4]

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14. ABSTRACT
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15. SUBJECT TERMS

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$$BV_{Actual} = 0.8 \times (BV_{PP}) \quad (1)$$

Since the actual breakdown voltage is only 80% of the parallel plane breakdown voltage, the parallel plane breakdown voltage was considered to be 1500V in order to obtain a breakdown voltage of 1200V. Equation 2 was used to calculate the required doping concentration of the drift region (N_{Drift}) to support the blocking voltage [4]. The drift region doping concentration was calculated to be 2.52 x 10^{16} cm^{-3}.

$$N_{Drift} = \left(\frac{3\times10^{15}}{BV_{PP}}\right)^{\frac{4}{3}} cm^{-3} \quad (2)$$

The drift region thickness (t_{Drift}) required to support the blocking voltage was calculated using equation 3 where ε_{SiC} is the relative permittivity of 4H-SiC and q is the electronic charge [4]. The calculated value corresponds to a thickness of 8.02 µm.

$$t_{Drift} = \sqrt{\frac{2\,\varepsilon_{SiC}\,BV_{PP}}{q\,N_{Drift}}} \quad (3)$$

The P-Base region doping had to be designed considering the breakdown voltage, threshold voltage and the on state resistance. The half cell was designed for a threshold voltage of 6V and the following equation was used to optimize the threshold voltage (V_{TH}) by varying the P-Base Region doping [4].

$$V_{TH} = \frac{t_{ox}}{\varepsilon_{ox}} \sqrt{4\,\varepsilon_{ox}\,k_b\,T_L\,N_A\,ln\left(\frac{N_A}{n_i}\right)} \quad (4)$$

In the above equation, ε_{ox} is the relative permittivity of silicon dioxide, k_b is the Boltzmann constant, the lattice temperature (T_L) and n_i is the intrinsic carrier concentration of 4H-SiC. For an oxide layer thickness (t_{ox}) of 30 nm, a P-Base region doping concentration (N_A) of 5.3 x 10^{17} cm^{-3} was calculated. The minimum thickness of P-Base region was calculated as 1.75 microns using equation 3. The calculated design parameters of the MOSFET had to be modified to obtain the required device characteristics. These modifications were made after several cycles of simulation and optimization. The drift region doping concentration was optimized to 2.1 x 10^{16} cm^{-3} and a value of 5 x 10^{17} cm^{-3} was used for the P-Base region doping concentration. The source and substrate regions were heavily doped to a concentration of 1 x 10^{19} cm^{-3}. Fig. 2 shows the contour plot of the net doping profile used for the half cell MOSFET structure. The D-MOSFET structure inherently gives rise to a parasitic NPN Bipolar Junction Transistor (BJT) between the Source region, the P-Base region and the Drift region where the source forms the emitter, the P-base region forms the base and the drain/substrate forms the collector. If this BJT turns ON, the gate will lose control over the drain current and the over-current can lead to device destruction. This process is called Latch-up [5]. In order to prevent this, the source electrode and the p-Base region are shorted together which in turn shorts the emitter and base of the parasitic BJT thus preventing latch-up.

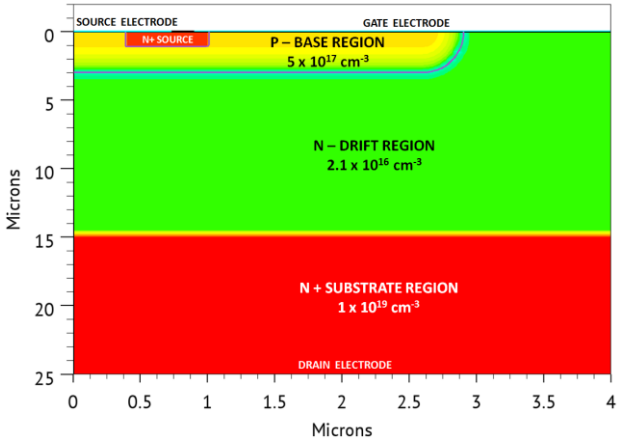

Figure 2. D-MOSFET half cell color coded net doping concentration profile (Green: Minimum Red: Maximum).

C. Half Cell Dimensions

The physical dimensions of the cell shown in fig. 3 were designed after referring to various designs and tradeoffs in [6]. The cell pitch for the half cell was selected as 4 microns, the width of the gate electrode was selected to be 3 microns which is the same as the width of the polysilicon window and the width of the contact window to N+ source and P-base region was 0.75 microns. The P-Base region width and depth was chosen to be 3 microns each which gave a desired channel length of 2 microns.

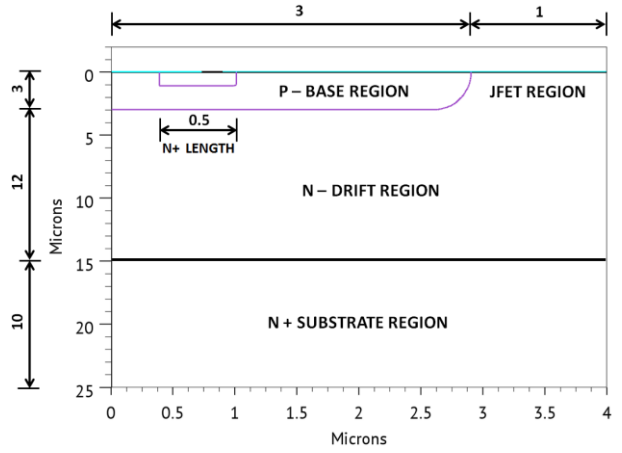

Figure 3. D-MOSFET half cell dimensions.

The JFET region width was a critical factor as less wide region would enhance the device breakdown by exhibiting field ring effect at the expense of on state resistance due to current constriction whereas a wider JFET region would result in lower on state resistance at the expense of breakdown at the p-base region edges. Considering these tradeoffs, the JFET region was selected to be 1 micron wide. The depth of the source and substrate regions was 1

micron and 10 microns respectively. The drift region thickness was optimized to 12 microns after several simulations.

D. Simulation Models

The accuracy of any physics based simulation depends upon the selection of models and the associated parameters. In this paper, the simulation of Silicon carbide assumed a defect free material. The recombination models included Shockley-Read-Hall (SRH) and Auger recombination [3]. Auger recombination model is applied to power device simulation due to the high current densities involved. Incomplete ionization model was selected due to the fact that the doping impurities in 4H-SiC have activation energies larger than the thermal energy ($k_B.T_L$) even at room temperature [3]. Due to high doping concentration in the source and substrate region, the effects of band gap narrowing were modeled using the band gap narrowing model available in Silvaco [3]. One of the most critical parameters in the modeling of MOSFET is the mobility. Mobility in a vertical D-MOSFET structure comprises of the vertical component through the bulk of the device and the horizontal component through the channel. The two major factors affecting mobility are phonon scattering and ionized impurity scattering. These effects were modeled using Caughey Thomas Analytic model and the velocity dependent mobility model [3]. The breakdown simulation was performed using Selberherr model which uses a modified Chynoweth law to calculate the impact generation rate [3]. Thermal simulations were performed using the GIGA module integrated into Silvaco ATLAS simulator which uses Wachutka's thermodynamic model of Lattice heating [3].

III. DC CHARACTERISTICS

A. Breakdown Simulation

The Breakdown simulation of wide band gap power devices is usually limited by the extremely low intrinsic carrier concentration. This issue is generally bypassed by artificially increasing the carrier concentration by high energy optical beam like laser. This can be avoided by using high precision option in the simulation software. The breakdown simulation (Fig. 4) for power MOSFET was performed using 128-bit extended precision. The use of high precision eliminates the issue of low carrier concentration by calculating the current density of the particles responsible for avalanche breakdown. The simulation was carried out at ambient temperatures of 23°C, 150°C and 250°C. Since holes have a higher impact ionization rate than electron in silicon carbide, the breakdown voltage almost remains constant even at elevated temperatures. This is due to the positive temperature coefficient of holes in case of silicon carbide as discussed in [7, 8]. The higher ambient temperature influences the leakage current through the device as depicted in fig. 4. A maximum electric field magnitude of 2.7 MV/cm^{-1} was observed during the breakdown simulation at 300K at the junction between the P-base region and the drift region.

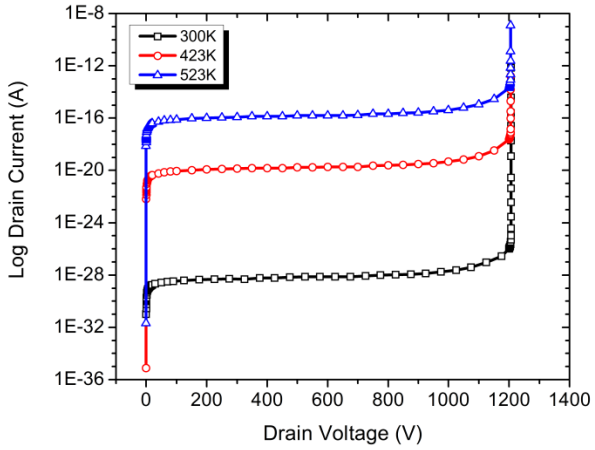

Figure 4. D-MOSFET half cell breakdown characteristics as a function of ambient temperature.

B. I_D vs. V_{DS} Characteristics

The device was simulated for its output characteristics at multiple gate voltage values. The family of curves was obtained for ambient temperature conditions of 23°C, 150°C and 250°C. The current voltage characteristics for the MOSFET at 300K ambient lattice temperature are shown in fig. 5. The gate voltage was varied linearly in steps of 1V starting from 8V till 15V to obtain the family of curves.

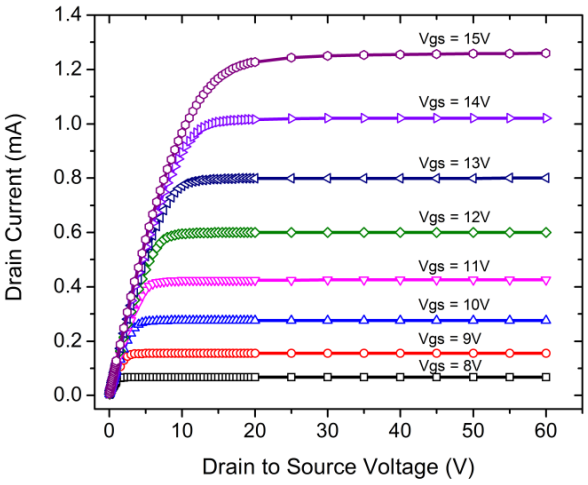

Figure 5. Current voltage characteristics at 300K ambient temperature.

IV. TRANSIENT ANALYSIS

The objective of this research was to analyze the effect of transient device current whose magnitude is much higher than the rated current. The device was pulsed for current densities five times and ten times the rated value with varying pulse widths. The purpose of varying the pulse width is to understand the power dissipation and lattice heating pattern at under these conditions.

A. RLC Ring Down Circuit

In the initial phase of transient analysis, the series RLC ring down circuit was simulated using PSPICE student version. In order to obtain a critically damped waveform, the combination of R, L and C should be selected such that the damping coefficient (ξ) is unity as per equation 5.

$$\xi_{RLC} = \frac{R}{2}\sqrt{\frac{C}{L}} \tag{5}$$

Fig. 6 shows the simplified circuit diagram used for generating the current pulse. The device under test (DUT) represents the half cell D-MOSFET.

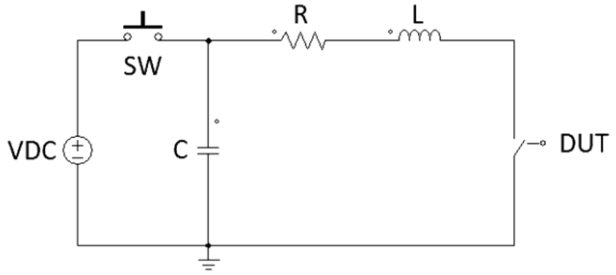

Figure 6. RLC ring down circuit (simplified).

B. Device Current Density

As per the design requirements, the rated current density of the MOSFET had to be 100A/cm^2. In ATLAS 2D simulations, the third dimension or the z-axis is by default 1 micron long [3]. This results in an unrealistically high current density because the area for vertical current flow devices is x (length) times the z (length). For the MOSFET half cell, the x is 4 microns long, y is 25 microns long and z is by default one micron. In Silvaco ATLAS, the z axis length can be altered to obtain the 3D effect [3]. The z axis length scales the terminal quantities like current, contact resistance etc.. When the device structure is analyzed for the current density distribution, the area used to calculate the current density, gets scaled by the value specified for the width parameter. Since the maximum current density is at the channel, the channel current density was monitored during the simulation while changing the value of z axis length. The z axis length at which the electron current density in the channel becomes 100A/cm^2 was used throughout the transient simulations.

C. MOSFET Turn ON

The gate of a MOSFET is isolated by an oxide layer from the rest of the semiconductor. During switching applications, the current required to charge/discharge the gate capacitor can be high depending upon the switching frequency and the magnitude of the gate capacitance. A simple analysis can be done using the basic capacitor equation

$$I_{Cap} = C\,\frac{dV}{dt} \tag{6}$$

If the voltage (V) across the capacitor (C) has to raised in a short interval of time (dt), the current (I_{Cap}) required will be very high. The capacitance of a MOSFET can be classified into Gate to Source Capacitance (C_{GS}), Gate to Drain or Miller Capacitance (C_{GD}) and Drain to Source Capacitance (C_{DS}) of the body diode. C_{GD} and C_{DS} are a function of Drain to Gate voltage and Drain to Source Voltage respectively. Since C_{GD} and C_{DS} are dependent on the width of space charge region, higher the voltage, lower the capacitance [9]. The gate to source voltage profile during MOSFET turn ON is shown in fig. 7. During time interval t_1 to t_2, the Gate to Source voltage starts rising from 0V to V_{TH} (in this case, 6V). The charge accumulated during this interval is Q_{GS} and is mainly used to energize C_{GS}.

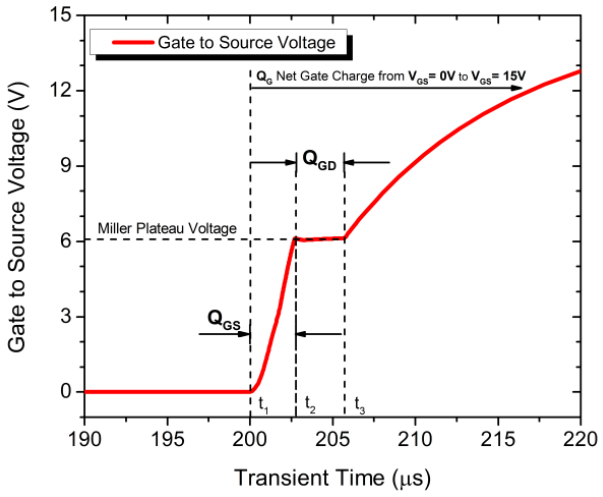

Figure 7. Gate to source voltage profile during MOSFET turn ON.

During time interval t_2 to t_3, the Gate to Source voltage remains at a constant voltage level known as Miller Plateau Voltage (V_{GP}). In the Miller Plateau region, the Gate to Source voltage waveform has zero slope. The presence of a slope indicates change in voltage and hence, current flow into C_{GS}. Since V_{GP} is a function of the on-state current density, in this simulation, the magnitude of V_{GP} and V_{TH} are almost the same since the current density is very low due to the nature of the circuit. Since Gate to Source voltage is constant, there is no current flow into C_{GS}. The charge accumulated during this interval is Q_{GD} and is used to energize capacitor C_{GD} [9]. After time t_3, the Gate to Source voltage again starts rising from Miller plateau to the final magnitude of the Gate voltage at a slower rate. This voltage is also known as overdrive

voltage as it is used to fully enhance the conducting channel of the MOSFET and further reduce the on-state resistance. In this regime, the net Gate charge is again shared between C_{GS} and C_{GD} [9].

D. 1000A/cm² Current pulse

The MOSFET was simulated for current pulses pertaining to current densities of 500 A/cm^2 and 1000 A/cm^2 for varying pulse widths at ambient temperatures of 300K. The half cell was simulated using a current pulse with peak magnitude of 1000 A/cm^2 and pulse width of 50 µs. Fig. 8 shows the drain voltage and current density waveforms. The current pulse had a di/dt of 0.8 A/µs measured between 10% and 90% of the total current density magnitude (in case of 1000A/cm^2, it was measured from 100 A/cm^2 to 900 A/cm^2). The higher magnitude current pulse was obtained modifying the charging voltage for the capacitor in the RLC ring down circuit.

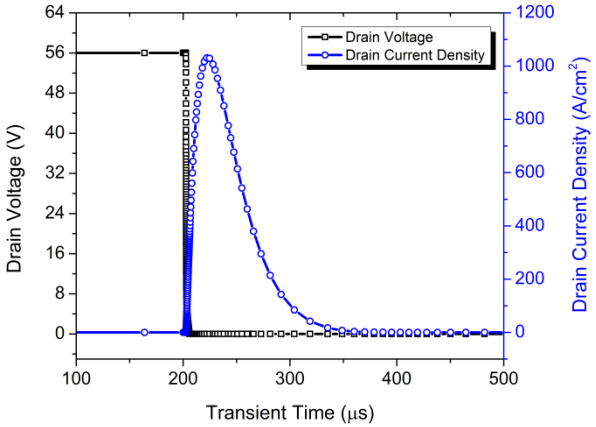

Figure 8. D-MOSFET voltage and current density waveforms for 1000 A/cm^2, 50 µs current pulse.

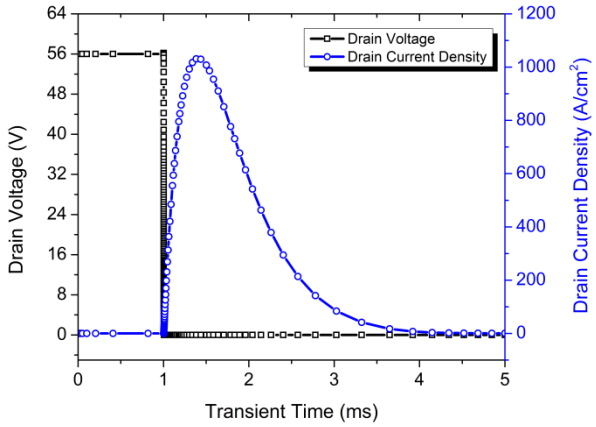

Figure 9. D-MOSFET voltage and current density waveforms for 1000 A/cm^2, 1 ms current pulse.

To analyze the conduction losses, the same current pulse was applied to the MOSFET but with a pulse width of 1 ms. Fig. 9 shows the drain voltage and current waveforms pertaining to a 1000 A/cm^2, 1 ms current pulse. The 1 ms pulse width was designed using a capacitor value of 200 µF and an inductance of 800 µH in the RLC ring down circuit.

E. Power Dissipation and Lattice Temperature

The power dissipation for any switching device is dependent on the voltage current overlap. As the switching frequency increases, the switching losses dominate over the conduction losses. Fig. 10 shows the MOSFET power dissipation and lattice temperature change pertaining to the 1000 A/cm^2, 1ms current pulse shown in fig. 9. It can be seen in fig. 10 that for a 1000 A/cm^2, 1ms current pulse, there is power dissipation at the turn on of the device but once the device turns on, the power dissipation is dominated by the ON state losses.

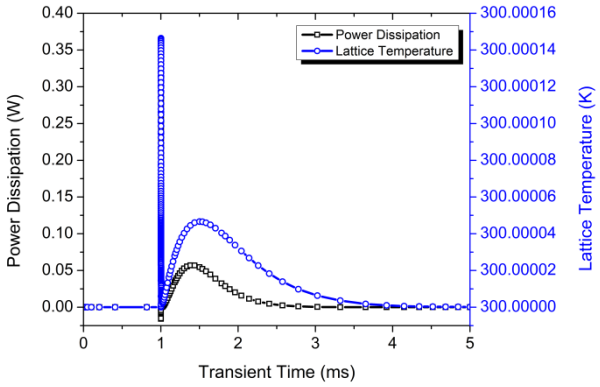

Figure 10. D-MOSFET power and lattice temperature waveforms for 1000 A/cm^2, 1 ms current pulse.

The energy in the pulse was obtained by integrating the power dissipation waveform. The power waveform for the 1000 A/cm^2, 1ms current pulse was integrated to obtain a total energy of 43 micro joules including conduction and switching losses. Table 1 shows the energy dissipation pattern for 1000 A/cm^2 current pulse for varying pulse widths at 300K ambient temperature.

Table 1. Energy Dissipation Summary for 1000A/cm^2 current pulse at 300K ambient temperature.

Pulse Width (µs)	Peak Power Dissipated (W)	Total Energy Dissipated (µJ)
50	5.7	14
100	2.9	10
200	1.45	11
500	0.58	22
1000	0.27	43

The fast switching capabilities of a MOSFET are due to the fact that only majority carriers i.e. electrons in an N-

channel MOSFET, are involved in conduction. The absence of minority carrier injection (unlike BJTs) facilitates the termination of device current almost instantly when the gate voltage is reduced below the threshold voltage. The switching characteristics of a device is dependent on the dielectric relaxation time (t_{dr}) which is defined as the characteristic time required by a semiconductor to reach electrical neutrality after carrier injection or extraction [10]. Dielectric relaxation time is given by the equation

$$t_{dr} = \frac{\varepsilon}{q\,N\,\mu} \tag{7}$$

Where ε is the relative permittivity, q is the magnitude of electronic charge, N is the doping concentration and μ is the mobility of the electron or hole depending on the particle considered. Typically for a MOSFET, the dielectric relaxation time is of the order of picoseconds which theoretically permit very high frequency switching [11]. However, the practical switching frequency is limited by the various capacitors formed internally in the device structure. The 2D simulation was performed on a half cell structure due to which the magnitude of capacitance in the device structure was so small that the change in drain to source voltage waveform during turn on had a steep slope. This caused a minimal overlap between the voltage and current resulting in minimum power dissipation as evident from the figures. The low power dissipation together with the high thermal conductivity resulted in a minuscule rise in temperature.

V. SUMMARY

A 2D model for 4H-SiC N-Channel D-MOSFET was designed using Silvaco ATLAS. The device breakdown characteristics were generated without artificially altering the intrinsic concentration of the material using 128-bit extended simulation precision. The device breakdown voltage did not get altered even at 250°C. The MOSFET characteristics including the Drain Current vs. Drain Voltage and transfer characteristics were verified at elevated ambient temperature. The Transient analysis of the VD-MOSFET was carried out using current pulses designed for five and ten times the rated current density of 100 A/cm^2 at 27°C ambient temperature conditions. The pulse width of the current pulses was varied to understand the transient performance. It was observed that as the ambient temperature increased, the conduction losses increased due to the increasing on state resistance. Under all the simulation conditions including the worst case power dissipation, the energy dissipated was not sufficient enough to raise the Lattice temperature of the device. This was primarily due to the rapid decrease in the drain to source voltage upon turn ON of the device which resulted in minimum overlap between voltage and current.

VI. REFERENCES

[1] Richmond, J; Hodge, S; Palmour, J.;, "Silicon Carbide Power Applications and Device Roadmap", *Power Electronics Europe*, Issue 7, 2004. 1

[2] Vasileska, Dragica, and Stephen M. Goodnick. "The Drift–Diffusion Equations and Their Numerical Solution." Computational Electronics. [San Rafael, Calif.]: Morgan & Claypool, 2006. 33-37. Print

[3] Silvaco© "ATLAS User's Manual", January 18, 2012. <http://www.Silvaco.com>

[4] Baliga, B. Jayant. "Power MOSFETs." Fundamentals of Power Semiconductor Devices. Berlin: Springer, 2008. 289-312. Print

[5] Dodge, Jonathan;, "Power MOSFET Tutorial", Advanced Power Technology. Application Note. APT-0403 Rev B. March 2, 2006. 1-12

[6] Baliga, B. Jayant. "Planar Power MOSFETs." Silicon Carbide Power Devices. New Jersey: World Scientific, 2005. 227-255. Print

[7] Baliga, B. Jayant. "Material Properties and Technology." Silicon Carbide Power Devices. New Jersey: World Scientific, 2005. 15-26. Print

[8] Raghunathan, R.; Baliga, B. Jayant; , "Measurement of electron and hole impact ionization coefficients for SiC," Power Semiconductor Devices and IC's, 1997. ISPSD '97., 1997 IEEE International Symposium on , vol., no., pp.173-176, 26-29 May 1997

[9] Balogh, Lazlo;, "Design And Application Guide For High Speed MOSFET Gate Drive Circuits", Texas Instruments Literature number slup169

[10] Kao, Kwan-Chi. "Electrical Conduction and Photoconduction." Dielectric Phenomena in Solids: With Emphasis on Physical Concepts of Electronic Processes. 1st ed. Amsterdam: Academic, 2004. 432-433. Print.

[11] Baliga, B. Jayant. "Power MOSFETs." Fundamentals of Power Semiconductor Devices. Berlin: Springer, 2008. 385-386. Print